I claim:

1. A capacitor comprising:

a first electrode;

a first dielectric coupled to the first electrode; and

a second electrode coupled to the first dielectric, wherein the second electrode includes an inhibiting layer that acts to enhance conductivity.

2. The capacitor of claim 1, wherein the inhibiting layer acts to inhibit formation of an undesired second dielectric.

3. The capacitor of claim 1, wherein the inhibiting layer acts to inhibit a diffusion that increases resistivity.

4. The capacitor of claim 1, wherein the inhibiting layer acts to inhibit a formation of an undesired oxidation compound so as to enhance an ohmic contact.

5. The capacitor of claim 1, wherein the second electrode is disposed as a top electrode of the capacitor.

6. The capacitor of claim 1, wherein the inhibiting layer includes a layer disposed on the second electrode.

7. The capacitor of claim 1, wherein the inhibiting layer includes a layer embedded in the second electrode.

8. The capacitor of claim 1, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a

nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal is selected from a group consisting of platinum, gold, titanium, and silver, and wherein the noble metal alloy is selected from a group consisting of graphite, chlorimet 3, and hastelloy C.

9. A capacitor comprising:

a first electrode that comprises at least one conductive metal oxide;

a dielectric coupled to the first electrode; and

a second electrode coupled to the dielectric, wherein the second electrode includes an inhibiting layer that inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

10. The capacitor of claim 9, wherein the at least one conductive metal oxide of the first electrode is selected from a group consisting of ruthenium oxide and iridium oxide.

11. The capacitor of claim 9, wherein the dielectric comprises at least one insulator metal oxide.

12. The capacitor of claim 11, wherein the at least one insulator metal oxide of the dielectric includes ditantalum pentaoxide.

13. The capacitor of claim 9, wherein the second electrode comprises at least one conductive metal oxide.

14. The capacitor of claim 13, wherein the at least one conductive metal oxide of the second electrode is selected from a group consisting of ruthenium oxide and iridium oxide.

15. The capacitor of claim 9, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy.

16. The capacitor of claim 15, wherein the transition metal of the inhibiting layer is selected from a group consisting of platinum, rhodium, and tungsten.

17. The capacitor of claim 15, wherein the transition metal alloy of the inhibiting layer includes a platinum rhodium alloy.

18. The capacitor of claim 15, wherein the nitride compound of the inhibiting layer is selected from a group consisting of tungsten nitride and titanium nitride.

19. A capacitor comprising:

a first electrode that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

a dielectric coupled to the first electrode, wherein the dielectric comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second electrode coupled to the dielectric, wherein the second electrode comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second electrode includes an inhibiting layer, wherein the

inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal is selected from a group consisting of platinum, gold, titanium, and silver, and wherein the noble metal alloy is selected from a group consisting of graphite, chlorimet 3, and hastelloy C.

20. The capacitor of claim 19, wherein the second electrode is disposed as a top electrode of the capacitor.

21. The capacitor of claim 19, wherein the inhibiting layer includes a layer disposed on the second electrode.

22. The capacitor of claim 19, wherein the inhibiting layer includes a layer embedded in the second electrode.

23. A semiconductor structure comprising:

an insulation layer that includes a first insulation substance; and

a first conductive layer abutting the insulation layer, wherein the first conductive layer includes an inhibiting layer that acts to enhance conductivity.

24. The semiconductor structure of claim 23, further comprising a second conductive layer abutting the insulation layer.

25. The semiconductor structure of claim 23, wherein the first conductive layer is adapted to receive electronic charges so as to allow the semiconductor structure to store desired information.

26. The semiconductor structure of claim 23, wherein the inhibiting layer includes a layer disposed on the first conductive layer.

27. The semiconductor structure of claim 23, wherein the inhibiting layer includes a layer embedded in the first conductive layer.

28. The semiconductor structure of claim 23, wherein the inhibiting layer inhibits a diffusion to form a second insulation substance.

29. The semiconductor structure of claim 23, wherein the inhibiting layer inhibits a diffusion that increases resistivity.

30. The semiconductor structure of claim 23, wherein the inhibiting layer includes a layer embedded in the first conductive layer.

31. The semiconductor structure of claim 23, wherein the inhibiting layer inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

32. A semiconductor structure comprising:

an insulation layer that comprises at least one insulator metal oxide; and

a first conductive layer abutting the insulation layer, wherein the first conductive layer includes an inhibiting layer that inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

33. The semiconductor structure of claim 32, further comprising a second conductive layer abutting the insulation layer.

34. The semiconductor structure of claim 32, wherein the at least one insulator metal oxide of the insulation layer includes ditantalum pentaoxide.

35. The semiconductor structure of claim 32, wherein the first conductive layer comprises at least one conductive metal oxide.

36. The semiconductor structure of claim 35, wherein the at least one conductive metal oxide of the first conductive layer is selected from a group consisting of ruthenium oxide and iridium oxide.

37. The semiconductor structure of claim 32, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy.

38. The semiconductor structure of claim 37, wherein the transition metal of the inhibiting layer is selected from a group consisting of platinum, rhodium, and tungsten.

39. The semiconductor structure of claim 37, wherein the transition metal alloy of the inhibiting layer includes a platinum rhodium alloy.

40. The semiconductor structure of claim 37, wherein the nitride compound of the inhibiting layer is selected from a group consisting of tungsten nitride and titanium nitride.

41. A semiconductor structure comprising:

an insulation layer that comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a first conductive layer abutting the insulation layer, wherein the first conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the first conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C..

42. The semiconductor structure of claim 41, further comprising a second conductive layer abutting the insulation layer.

43. The semiconductor structure of claim 41, wherein the first conductive layer is adapted to receive electronic charges so as to allow the semiconductor structure to store desired information.

44. The semiconductor structure of claim 41, wherein the inhibiting layer includes a layer disposed on the first conductive layer.

45. The semiconductor structure of claim 41, wherein the inhibiting layer includes a layer embedded in the first conductive layer.

46. A semiconductor structure comprising:

a first conductive layer that comprises at least one conductive metal oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy , wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C.

47. The semiconductor structure of claim 46, wherein the at least one conductive metal oxide of the first conductive layer is selected from a group consisting of ruthenium oxide and iridium oxide.

48. The semiconductor structure of claim 46, further comprising a metallization layer abutting the first conductive layer.

49. The semiconductor structure of claim 48, wherein the metallization layer includes a diffusion barrier.

50. The semiconductor structure of claim 48, further comprising an insulation layer abutting the first conductive layer, wherein the insulation layer includes a first insulation substance.

51. A memory cell comprising:

a capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer.

52. The memory cell of claim 51, wherein the gate of the at least one transistor is adapted to receive an access signal to selectively access the capacitor.

53. A memory array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer.

54. A memory device comprising:

an array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer; and

an address decoder;

a row access circuitry;

a column access circuitry;

a controller; and

an input/output circuit.

55. A circuit module comprising:

a plurality of dies, wherein at least one die comprises:

at least one array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum

rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer; and

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control.

56. A memory module comprising:

a plurality of memory devices, wherein at least one memory device comprises:

at least one array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one

conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer; and

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal; and

a plurality of data links coupled to the plurality of memory devices to communicate data.

57. An electronic system comprising:

a plurality of circuit modules comprising:

a plurality of dies, wherein at least one die comprises:

at least one array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one

conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

and

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control; and

a user interface.

58. A memory system comprising:

a plurality of memory modules comprising:

a plurality of memory devices, wherein at least one memory device comprises:

at least one array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide, wherein the second conductive layer includes an inhibiting layer, wherein the inhibiting layer comprises a substance selected from a

group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet 3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer; and

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data; and

a memory controller.

59. A computer system comprising:

a processor;

a memory system comprising:

a plurality of memory modules comprising:

a plurality of memory devices, wherein at least one memory device comprises:

at least one array of memory cells, the array comprising:

at least one capacitor that includes:

a first conductive layer that comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide; and

a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal includes platinum, gold, titanium, and silver, and wherein the noble metal alloy includes graphite, chlorimet

3, and hastelloy C; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer; and

at least one bulk storage device.

60. A method of forming a semiconductor structure, the method comprising:

forming a first conductive layer;

forming an insulation layer abutting the first conductive layer;

forming a second conductive layer abutting the insulation layer; and

forming an inhibiting layer abutting the second conductive layer, wherein the inhibiting layer inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

61. The method of claim 60, wherein forming the inhibiting layer includes forming the inhibiting layer on the second conductive layer.

62. The method of claim 60, wherein forming the inhibiting layer includes embedding the inhibiting layer in the second conductive layer.

63. The method of claim 60, wherein the method does not proceed in the order presented.

64. The method of claim 60, wherein forming the first conductive layer includes forming the first conductive layer from at least one conductive metal oxide.

65. The method of claim 64, wherein forming the first conductive layer includes forming the first conductive layer from the at least one conductive metal that is selected from a group consisting of ruthenium oxide and iridium oxide.

66. A method of forming a semiconductor structure, the method comprising:

forming a first conductive layer, wherein forming the first conductive layer includes forming the first conductive layer from at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming an insulation layer abutting the first conductive layer, wherein the insulation layer includes at least one insulator metal oxide;

forming a second conductive layer abutting the insulation layer; and

forming an inhibiting layer abutting the second conductive layer, wherein the inhibiting layer inhibits formation of an undesired oxidation compound so as to enhance an ohmic contact.

67. The method of claim 66, wherein forming the insulation layer includes forming from the at least one insulator metal oxide that includes ditantalum pentaoxide.

68. The method of claim 66, wherein forming the second conductive layer includes forming from at least one conductive metal oxide.

69. The method of claim 68, wherein forming the second conductive layer includes forming from the at least one conductive metal oxide that is selected from a group consisting of ruthenium oxide and iridium oxide.

70. The method of claim 66, wherein forming the inhibiting layer includes forming the inhibiting layer from a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy.

71. The method of claim 70, wherein forming the inhibiting layer includes forming from the transition metal that is selected from a group consisting of platinum, rhodium, and tungsten.

72. The method of claim 70, wherein forming the inhibiting layer includes forming from the transition metal alloy that includes a platinum rhodium alloy.

73. The method of claim 70, wherein forming the inhibiting layer includes forming from the nitride compound that is selected from a group consisting of tungsten nitride and titanium nitride.

74. A method of forming a semiconductor structure, the method comprising:

forming a first conductive layer, wherein the first conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming an insulation layer abutting the first conductive layer, wherein the

insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide;

forming a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide; and

forming an inhibiting layer abutting the second conductive layer, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal is selected from a group consisting of platinum, gold, titanium, and silver, and wherein the noble metal alloy is selected from a group consisting of graphite, chlorimet 3, and hastelloy C.

75. The method of claim 74, further comprising forming a diffusion barrier abutting to the second conductive layer.

76. The method of claim 75, wherein forming a diffusion barrier includes forming from a group selected from a nitride compound, a carbide compound, a boride compound, a transition metal alloy, and a transition metal nitride compound alloy.

77. The method of claim 76, wherein forming the diffusion barrier includes forming from the nitride compound that includes titanium nitride.

78. The method of claim 76, wherein forming the diffusion barrier includes forming from the transition metal alloy that includes titanium tungsten.

79. The method of claim 76, wherein forming the diffusion barrier includes forming from the transition metal nitride compound alloy that includes titanium nitride tungsten.

80. A method of forming a semiconductor structure, the method comprising:

forming a first conductive layer, wherein the first conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming an insulation layer abutting the first conductive layer, wherein the insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide;

forming a second conductive layer abutting the insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming an inhibiting layer abutting the second conductive layer,wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, and wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal is selected from a group consisting of platinum, gold, titanium, and silver, and wherein the noble metal alloy is selected from a group consisting of graphite, chlorimet 3, and hastelloy C; and

forming a metallization layer abutting the inhibiting layer, wherein the metallization layer comprises a representative metal, and wherein forming the metallization layer further includes;

forming a diffusion barrier abutting the first conductive layer, wherein the diffusion barrier comprises a nitride compound, a carbide compound, a boride compound, a transition metal alloy, and a transition metal nitride compound alloy, wherein the nitride compound includes titanium nitride, wherein the transition metal alloy includes titanium tungsten, wherein the transition metal nitride compound alloy includes titanium nitride tungsten.

81. The method of claim 80, wherein forming a metallization layer includes forming from the representative metal that includes aluminum.

82. The method of claim 80, further comprising forming a silicide contact on a substrate.

83. The method of claim 82, wherein the method proceeds in the order presented.

84. The method of claim 80, further comprising:

forming an ohmic contact on a region of a substrate, wherein forming the ohmic contact includes forming the ohmic contact using a technique selected from a group consisting of doping the region of the substrate and forming a refractory metal silicide in the region of the substrate.

85. A method of forming a semiconductor structure, the method comprising:

forming an ohmic contact on a region of a substrate;

forming a first conductive layer, wherein the first conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming a first insulation layer abutting the first conductive layer, wherein the first insulation layer comprises at least one insulator metal oxide, wherein the at least one insulator metal oxide includes ditantalum pentaoxide;

forming a second conductive layer abutting the first insulation layer, wherein the second conductive layer comprises at least one conductive metal oxide, wherein the at least one conductive metal oxide is selected from a group consisting of ruthenium oxide and iridium oxide;

forming an inhibiting layer abutting the second conductive layer, wherein forming the inhibiting layer includes forming the inhibiting layer that includes the execution of a vapor deposition technique, wherein the vapor deposition technique is selected from a group consisting of physical vapor deposition and chemical vapor deposition, wherein the inhibiting layer comprises a substance selected from a group consisting of a transition metal, a transition metal alloy, a nitride compound, a noble metal, and a noble metal alloy, wherein the transition metal alloy includes a platinum rhodium alloy, wherein the transition metal is selected from a group consisting of platinum, rhodium, and tungsten, wherein the nitride compound is selected from a group consisting of tungsten nitride and titanium nitride, wherein the noble metal is selected from a group consisting of platinum, gold, titanium, and silver, and wherein the noble metal alloy is selected from a group consisting of graphite, chlorimet 3, and hastelloy C;

forming a second insulation layer abutting the inhibiting layer and the ohmic contact; and

forming a metallization layer abutting a diffusion barrier, wherein the metallization layer comprises a representative metal, wherein the representative metal includes aluminum, and wherein forming the metallization layer includes;

forming the diffusion barrier abutting the first conductive layer, wherein forming the diffusion barrier includes exposing the inhibiting layer and the ohmic contact through the second insulation layer, wherein the diffusion barrier comprises a nitride compound, a carbide compound, a boride compound, a transition metal alloy, and a transition metal nitride compound alloy, wherein the nitride compound includes titanium nitride, wherein the transition metal alloy includes titanium tungsten, wherein the transition metal nitride compound alloy includes titanium nitride tungsten.

86. The method of claim 85, wherein forming the inhibiting layer includes forming the inhibiting layer on the second conductive layer.

87. The method of claim 85, wherein forming the inhibiting layer includes embedding the inhibiting layer in the second conductive layer.